

J1036 U.S. P.P.  
09/886577  
06/21/01

	Class	Subclass
ISSUE CLASSIFICATION		

**U.S. UTILITY Patent Application**

<b>O.I.P.E.</b> <i>CC</i> <b>SCANNED</b> <i>TRJ</i> <b>Q.A.</b> <i>EW</i>	<b>PATENT DATE</b>
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APPLICATION NO. 09/886577	CONT/PRIOR	CLASS 365	SUBCLASS	ART UNIT 2818	EXAMINER
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## APPLICANTS

Richard Roy

**THE**

Simultaneous access and cache loading in a hierarchically organized memory circuit

ISSUING CLASSIFICATION											
ORIGINAL				CROSS REFERENCE(S)							
CLASS		SUBCLASS		CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)						
INTERNATIONAL CLASSIFICATION											

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	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)		<b>NOTICE OF ALLOWANCE MAILED</b>	
	<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____ _____ _____			
<b>ISSUE FEE</b>				
<input type="checkbox"/> The terminal ____ months of this patent have been disclaimed.	_____ (Primary Examiner) _____ (Date)		Amount Due	Date Paid
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